AMENDMENTS TO THE SPECIFICATION:

Replace the paragraph beginning at page 29, line 1, with the following rewritten paragraph:

--Then, as shown in Figs. 1B and 12B, a patterned resist 6 having a slit-shaped diffusion layer-pattern is formed via a known lithography technology on the HTO or LTO 5 (or on the silicon layer 4 if no HTO or LTO 5 is disposed thereon). In Fig. 12B, the ~~doted~~ dotted defines device isolation region. Here, the above-mentioned method described in the earlier application includes depositing the silicon nitride film 16 on the silicon layer 4 before forming the patterned resist 6, and a stress created by a different in the coefficient of thermal expansion between the silicon layer 4 and the silicon nitride film 16 is utilized to inhibit the growth of the bit-line oxide 13, as shown Figs. 11. On the contrary, the method according to [[the]] this embodiment does not require forming the bit-line oxide 13, and thus the deposition of the silicon nitride film 16 can be eliminated from the manufacturing process, and thus providing more simplified manufacturing process in comparison with the method described in the earlier application.--